70. A non-volatile memory circuit as recited in claim 67 including multiple sets of said memory cells, each set having a respective common drive line thereby forming a memory circuit matrix comprising rows and columns of said memory cells.

71. A non-volatile memory circuit as recited in claim 67 including respective means for isolating said sense amplifier from the corresponding bit lines.

REMARKS

The amendments to the specification are for the purpose of carrying over changes made to the originally-filed parent application. The claims newly presented in this continuation application are substantially similar to those previously prosecuted in U. S. Patent Application Serial No. 377,170, filed July 10, 1989.

Respectfully submitted,

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